SCXI™

SCXIbus System Specification

Signal Conditioning eXtensions for Instrumentation System Specification

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The following conventions are used in this manual:

This icon denotes a note, which alerts you to important information.

bold Bold text denotes items that you must select or click on in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

`monospace` Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

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SCXIbus System Specification

Introduction

Scope

The Signal Conditioning eXtensions for Instrumentation bus (SCXIbus) is a multifunction bus that provides a serial communication bus, analog buses, trigger buses, and power to signal conditioning modules. The SCXIbus integrates many different signal conditioning functions into a single system that can be remotely configured and controlled.

Objectives

This specification describes the physical, electrical, and timing requirements for the SCXIbus. The system objectives of the SCXIbus specification are as follows:

- To specify the system characteristics that allow a module to control other modules or be controlled via the serial bus
- To specify the electrical and mechanical system characteristics required to design modules that will operate in the SCXIbus system

The *Physical Requirements* section describes the physical dimensions of an SCXI module, the positioning of the metral SCXIbus connector, and cooling information. The *SCXIbus Connector* section contains the pinout and a brief description of the SCXIbus backplane lines and requirements for module connections to these lines. The *Timing Requirements and Specifications* section contains a complete description and specification of the serial communications protocol and SCANCON timing.

Physical Requirements

This section discusses the physical dimensions of an SCXI module, the positioning of the metral SCXIbus connector, and cooling information. Figure 1 shows the physical dimensions for an SCXI module.

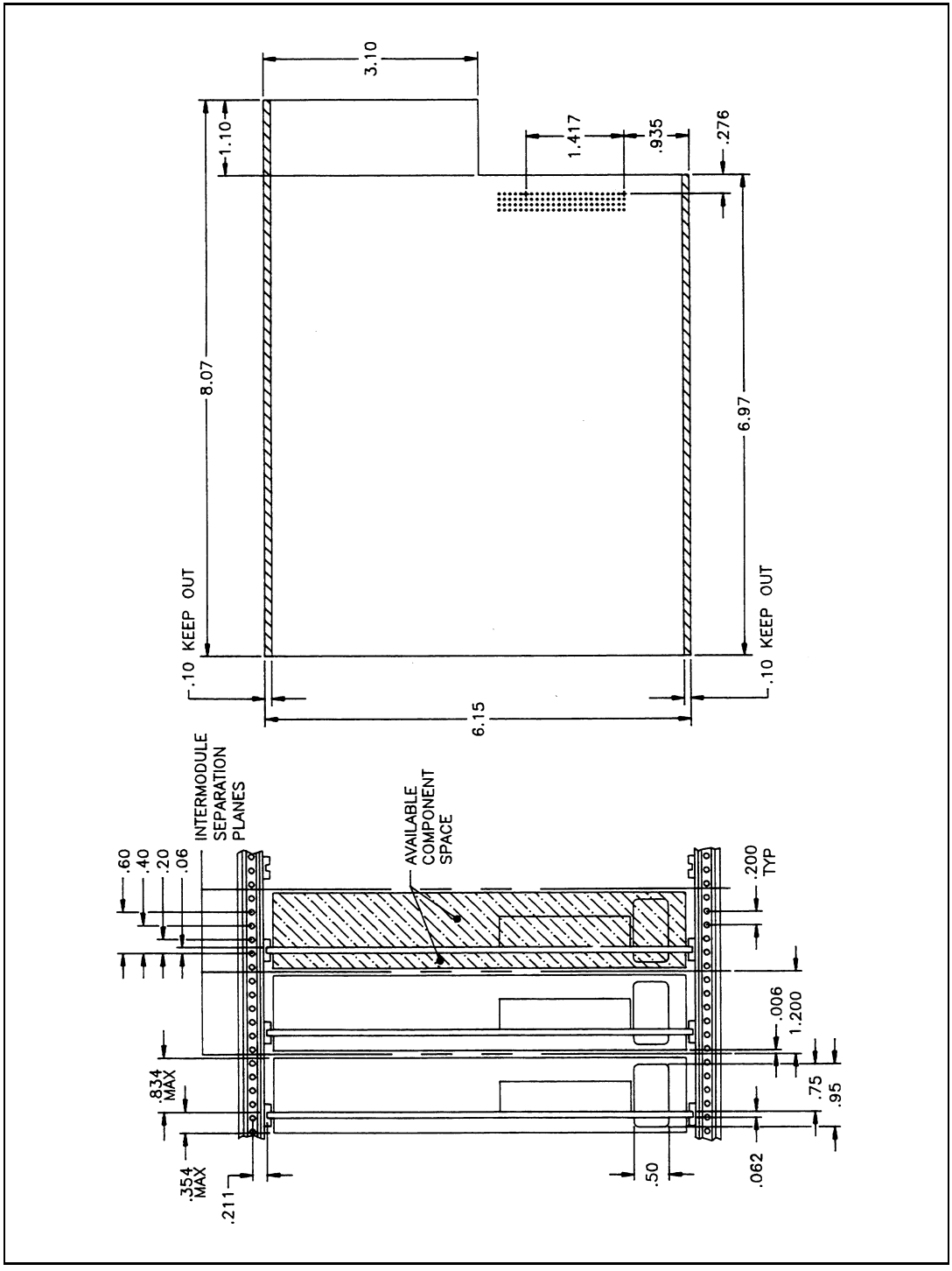


Figure 1. Dimensions for an SCXI Module

Module Dimensions

A module slides into the chassis on the plastic module guides. The edges of the module should be 0.062 in. thick to fit within the module guides. The module needs a keep-out area of 0.1 in. on the top and bottom of the module to keep components from rubbing against the module guides.

The module should be 6.15 in. high. The width limitations on a module are that no part of the module should come within 0.006 in. of the intermodule separation plane. For a properly aligned module, this equals a component height restriction of 0.834 in. on the top side of the board and 0.354 in. on the bottom side of the board. Notice that the component height restriction on the bottom side includes the thickness of the printed circuit board.

The depth of the module (distance front to back) should be 6.97 in. The module can extend 1.10 in. further back in the region that is no more than 3.1 in. from the top edge of the module. Because the metral connector does not have a large extraction force, you should mechanically secure the module to the chassis by using the top and bottom front-threaded strips.

Connector Position

The SCXIbus connector can be two 4x6 right-angle female metral connectors or one 4 x 24-pin right-angle female metral connector.

Table 1 shows the manufacturer part numbers National Instruments uses for the right-angle female metral connectors.

Table 1. Right-Angle Female Metral Connector Part Numbers

Size	Manufacturer	Part Number
4 x 6	DuPont	70268-901
4 x 24	DuPont	70270-901

Threaded Strip Holes

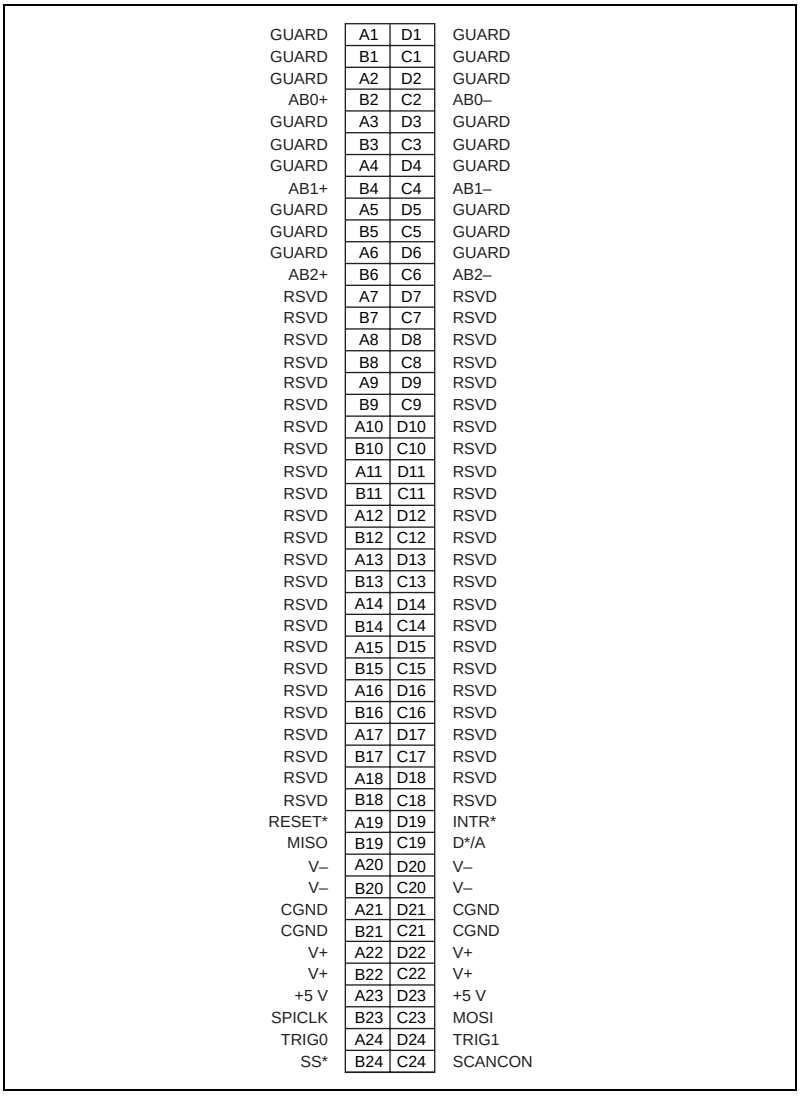
To secure a module to the chassis, use the threaded strips located on the front of the chassis and the two threaded strips on the rear of the chassis. The strips have 2.5 mm tapped holes on 0.2 in. spacing. The centers of these holes are 0.211 in. from the top and bottom edges of the module, and 0.20 in. from the top side of the module. A module can also use the holes that are 0.40 in., 0.60 in., and –0.06 in. from the top side of the module. The other two positions are reserved for set screws that secure the threaded strips to the chassis. The front and rear edges of the module coincide with the lip (the two flat spots on either side of a threaded strip) of the chassis.

Airflow Region

Airflow to the modules comes through a 0.5 in. by 0.95 in. hole in the backplane. Figure 1 shows the extent of this hole. If a module is dissipating more than a couple of watts of power, be sure that airflow is not inhibited. Air should circulate through the module and exit through the rear connector space.

SCXIbus Connector

The SCXIbus connector supplies power to the module. It also supplies access to the digital bus, analog buses, trigger lines, and selection signals. The SCXIbus connector is a subset of the 96-pin male metral header. Only the top and bottom 24 pins are used. The functions of the middle 48 pins are reserved for future products. A module uses a right-angle female metral connector for the mating connector. You can use either a 96-pin connector or two appropriately placed 24-pin connectors. Figure 2 shows the pin assignment of the SCXIbus connector.



GUARD	A1	D1	GUARD
GUARD	B1	C1	GUARD
GUARD	A2	D2	GUARD
AB0+	B2	C2	AB0–
GUARD	A3	D3	GUARD
GUARD	B3	C3	GUARD
GUARD	A4	D4	GUARD
AB1+	B4	C4	AB1–
GUARD	A5	D5	GUARD
GUARD	B5	C5	GUARD
GUARD	A6	D6	GUARD
AB2+	B6	C6	AB2–
RSVD	A7	D7	RSVD
RSVD	B7	C7	RSVD
RSVD	A8	D8	RSVD
RSVD	B8	C8	RSVD
RSVD	A9	D9	RSVD
RSVD	B9	C9	RSVD
RSVD	A10	D10	RSVD
RSVD	B10	C10	RSVD
RSVD	A11	D11	RSVD
RSVD	B11	C11	RSVD
RSVD	A12	D12	RSVD
RSVD	B12	C12	RSVD
RSVD	A13	D13	RSVD
RSVD	B13	C13	RSVD
RSVD	A14	D14	RSVD
RSVD	B14	C14	RSVD
RSVD	A15	D15	RSVD
RSVD	B15	C15	RSVD
RSVD	A16	D16	RSVD
RSVD	B16	C16	RSVD
RSVD	A17	D17	RSVD
RSVD	B17	C17	RSVD
RSVD	A18	D18	RSVD
RSVD	B18	C18	RSVD
RESET*	A19	D19	INTR*
MISO	B19	C19	D*/A
V–	A20	D20	V–
V–	B20	C20	V–
CGND	A21	D21	CGND
CGND	B21	C21	CGND
V+	A22	D22	V+
V+	B22	C22	V+
+5 V	A23	D23	+5 V
SPICLK	B23	C23	MOSI
TRIG0	A24	D24	TRIG1
SS*	B24	C24	SCANCON

Figure 2. SCXI Chassis SCXIbus Connector Pin Assignment

SCXIbus Connector Signal Descriptions

Pin	Signal Name	Description
B2	AB0+	Analog Bus 0+ —Positive analog bus 0 line.
C2	AB0–	Analog Bus 0– —Negative analog bus 0 line.
B4	AB1+	Analog Bus 1+ —Positive analog bus 1 line.
C4	AB1–	Analog Bus 1– —Negative analog bus 1 line.
B6	AB2+	Analog Bus 2+ —Positive analog bus 2 line.
C6	AB2–	Analog Bus 2– —Negative analog bus 2 line.
A1, B1, C1, D1, A2, D2, A3, B3, C3, D3, A4, D4, A5, B5, C5, D5, A6, D6	GUARD	Guard—Connect to one guard that shields and guards the analog bus lines from noise.
A19	RESET*	Reset—Control signal activated by the reset button on the front panel of Slot 0.
B19	MISO	Master-In-Slave-Out—One of two data lines on the digital bus. Used as data input by the master.
C19	D*/A	Data/Address—Used by the master to indicate to the slave the type of information that is being sent.
D19	INTR*	Interrupt—Active low. Causes data that is on MOSI to be written to the Slot-Select Register in Slot 0.
A20, B20, C20, D20	V–	Negative Analog Supply— –18.5 to –25 V.
A21, B21, C21, D21	CGND	Chassis Ground—Digital and analog ground reference.
A22, B22, C22, D22	V+	Positive Analog Supply— +18.5 to +25 V.
A23, D23	+5 V	+5 VDC Source—Digital power supply.
B23	SPICLK	Serial Peripheral Interface (SPI) Clock—Clocks the serial data on the MOSI and MISO lines.
C23	MOSI	Master-Out-Slave-In—One of two data lines on the digital bus. Used as data input by the slave.

Pin	Signal Name	Description
A24	TRIG0	TRIG0—General-purpose trigger line. Also used to send a clock signal to Slot 0 and other modules during hardware scanning.
B24	SS*	Slot Select—Indicates to a module that it has been selected as the slave.
C24	SCANCON	Scanning Control—Real-time selection line, typically used in module multiplexing to determine which module is being accessed in a scanned data acquisition.
D24	TRIG1	TRIG1—General-purpose trigger line.
* Indicates active low.		

All other pins are reserved for future use.

Electrical Requirements

Power Requirements

The V+, V–, and +5 V pins supply power to a module. Table 2 shows the specifications for the V+, V–, and +5 V lines.

Table 2. Power Specifications

Supply	Range	Ripple
V+	18.5 to 25 V	1.5 V peak-to-peak
V–	–18.5 to –25 V	1.5 V peak-to-peak
+5 V	4.75 to 5.25 V	50 mV peak-to-peak

All voltages are referenced to chassis ground.

Table 3 shows the current ratings for the SCXI-1000, SCXI-1000DC, and SCXI-1001 chassis.

Table 3. Supply Ratings

Supply	Current Rating		
	SCXI-1000	SCXI-1000DC	SCXI-1001
V+	680 mA	1.00 A	2.04 A
V–	680 mA	860 mA	2.04 A
+5 V	200 mA	1.60 A	600 mA

This averages to 170 mA of V+ and V– per slot and 50 mA of +5 V per slot for the SCXI-1000 and SCXI-1001 and 250 mA of V+, 215 mA of V– and 400 mA of +5 V for the SCXI-1000DC. A slot can use more than its share of the current, and it may use all of the available power. The total current rating for the chassis should not be exceeded, however. Due to thermal considerations, it is recommended that the modules should not dissipate more than 9 W. The current rating for the metral connector is 1 A per pin. Designers of high-power modules should be careful not to exceed this rating. Keep in mind that the current does not distribute itself equally among all pins. Use all four V+, V–, and CGND pins.

The V+ and V– supplies are fused on the backplane at 1 1/2 A on the SCXI-1000, at 2 A on the SCXI-1000DC, and at 4 A on the SCXI-1001. Fuse modules, especially experimental modules, at a lower current value appropriate to their expected current draw. For procedures on backplane fuse testing and replacement, refer to Chapter 2, *Configuration and Installation* of the *SCXI-1000/1000DC/1001 User Manual*.

Analog Buses and Guard

The three analog buses are connected to all modules, but not Slot 0. The analog buses are differential traces that any module can use to send or receive analog signals. The buses are shielded or guarded by the guard trace, which surrounds all the analog buses. The guard is floating on the backplane, so one module should tie it to a reference voltage, typically grounding it. No arbitration scheme exists for the analog bus, so you should output-protect to ±25 V any module that drives the bus.

Open-Collector Lines

The two trigger buses, TRIG0 and TRIG1, and the digital bus signals, MOSI, MISO, SPICLK, D*/A, and INTR*, are open-collector lines. On the SCXI-1000, the open-collector lines are pulled up on the backplane to +5 V with 2.2 kΩ resistors. On the SCXI-1001 chassis, the open-collector lines are pulled up on the backplane to +5 V with 1.2 kΩ resistors.

Open-collector or open-drain drivers, like the HCT05 and HCT03 chips, must drive the open-collector lines. A module should have a capacitive load of no more than 20 pF on these lines.

Because the open-drain drivers do not drive the lines high, rise times can be slow—up to 250 ns of delay for a gate threshold of 2 V. Slow edges can cause multiple transitions caused by noise pickup if you use normal gates to receive these lines. Therefore, a module using these lines as inputs should buffer each line with a schmidt trigger gate and keep the trace length from the SCXIbus connector to the gate under 2 in., avoiding close parallel paths with other digital traces. The delay caused by the rising edge varies with the system configuration and threshold levels of specific gates. Therefore, you should use only the falling edge of the trigger lines for critical timing functions.

Module drive requirements referenced to CHSGND are as follows:

- V_{OL} volts, output low 0.4 V max
- I_{in} input current at V_{OL} 5 mA max

HCT Input Lines

SS*, SCANCON, and RESET* are high-speed CMOS TTL (HCT) totem pole lines driven by Slot 0 and used as inputs by modules. SS* and SCANCON are unique to each module—for example, an SCXI-1000 chassis has four SS* and SCANCON lines. One line buses RESET* to all modules.

- A module may place up to 10 transistor-transistor logic (TTL) loads each on the SS* and SCANCON lines.
- A module may place 1 TTL load on the RESET* line.

Digital output specifications of Slot 0, referenced to CHSGND:

- V_{OH} volts, output high 3.7 V min at 4 mA max
- V_{OL} volts, output low 0.4 V max at 4 mA max

Timing Requirements and Specifications

This section describes the timing requirements and specifications for the SCXIbus signals.

RESET* Timing Requirements and Specifications

The RESET* signal shifts from low to high shortly after power up. Whenever you press the Reset Button on the front panel of Slot 0, the RESET* signal will be low. Within 10 µs after the rising edge of RESET*, the Module ID should be readable.

Digital Bus Timing Requirements and Specifications

This section describes the timing requirements and specifications for the digital bus communications signals.

Overview

Communication over the digital bus involves two parties. On the SCXI chassis, the master is a module and the slave is either another module or Slot 0. (Future SCXI chassis may only allow Slot 0 to be a master. In this case, Slot 0 would have a communications port—RS-232, GPIB, and so on.) The master module controls the INTR* and D*/A lines, supplies a serial clock on the SPICLK line, and supplies data to the slave on the MOSI line. The slave uses its SS* line, or INTR* line in the case of the Slot-Select Register, to determine incoming communications. It monitors the D*/A line to determine whether the information being sent on MOSI is a chip address or data. The slave may also send data back to the master through the MISO line, clocked by the master supplied SPICLK.

MOSI is an open-collector line that carries the data from the master module to either Slot 0 or a slave module.

MISO is an open-collector line that carries the data from the slave module to the master module. Notice that Slot 0 does not write information to this line, so during writes to Slot 0, the MISO line is always high.

SPICLK is an open-collector line that is driven by the master to clock the data on both the MOSI and MISO lines.

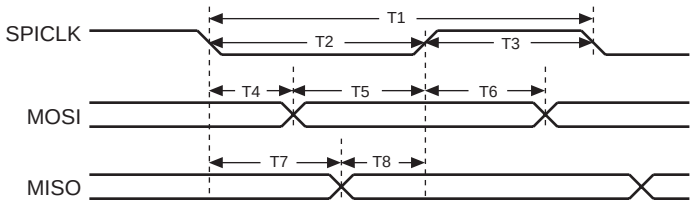
INTR* is an open-collector line that is driven by the master. When driven low, all SS* lines become inactive and the data on the MOSI line is written to the Slot-Select Register in Slot 0. The value written to the Slot-Select Register determines which module SS* line becomes active when the master releases INTR* high again. In the case of the SCXI-1001, the value written to the Slot-Select Register is also checked against the chassis address. If the numbers do not match, no SS* line becomes active when the master releases INTR*.

D*/A is an open-collector line that is driven by the master. When driven low, D*/A indicates to a module that information on MOSI is data. When driven high, D*/A indicates that information on MOSI is address information.

The SCXIbus connector provides access to these lines. To be a master, a module must be able to control the lines itself, or it needs to be cabled to something with a digital port that can supply the appropriate signals. You must convert the digital port signals to open-collector on the module to avoid overloading the open-collector backplane lines.

MOSI, MISO, and SPICLK Timing

SPICLK is an idle high-clock signal. When SPICLK falls low, this signals to the slave that the master is putting out data on MOSI. A low SPICLK signal also indicates that the slave should get data ready on the MISO line for the master to read. When SPICLK rises again, the master reads the MISO line, and the slave reads the data present on the MOSI line. Figure 3 shows the timing requirements for the master and slave.



Name	Description	Master	Slave
T1	Period of SPICLK	1.0 µs min	1.0 µs min
T2	Low time of SPICLK	450 ns min	450 ns min
T3	High time of SPICLK	450 ns min	200 ns min
T4	Delay from falling SPICLK to MOSI valid	50 ns min	—
T5	Time of MOSI valid before rising SPICLK	—	150 ns min
T6	Time of MOSI valid after rising SPICLK	400 ns min	150 ns min
T7	Delay from falling SPICLK to MISO valid	100 ns min	—
T8	Time of MISO valid before rising SPICLK	100 ns min	—

Figure 3. Master and Slave Timing Diagram

A slave maintains its MISO state until a new falling edge on SPICLK occurs. In addition, a slave must stop driving MISO low within 100 ns after Slot 0 disables SS*.

Slot-Select Procedure

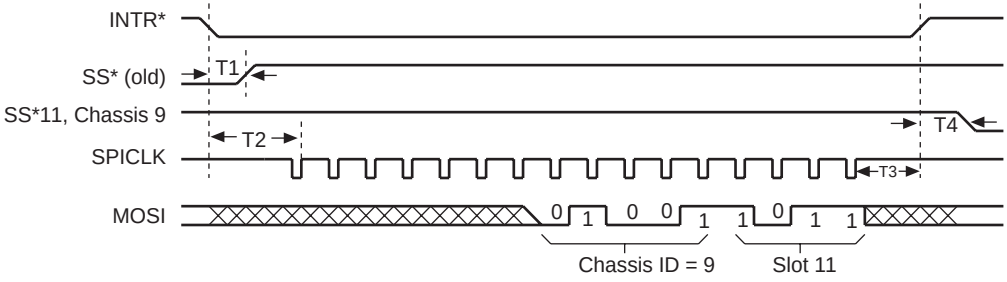
For a master to talk to another module, activate the module SS* line by writing a slot-select number to the Slot-Select Register in Slot 0. The INTR* line is like a SS* line for the Slot-Select Register. When INTR* is pulled low by the master, Slot 0 disables all SS* lines to all modules and reads any data clocked on the MOSI line into the Slot-Select Register. Data written to the Slot-Select Register is 16 bits long. After the 16 bits have been written, the master module releases INTR* high, causing Slot 0 to assert the SS* line of the specified slot. On the SCXI-1001, Slot 0 assets SS* only if the chassis number determined by the jumper settings and the chassis number written to the Slot-Select Register match. This procedure follows and corresponds to the timing diagram in Figure 4, which illustrates the case of selecting Slot 11 in Chassis 9.

1. Initial conditions:

   MOSI = don’t care
   D*/A = don’t care
   INTR* = high
   SPICLK = high

2. Pull INTR* low to deassert all SS* lines to all modules.
3. Release D*/A high.

4. For each bit, starting with the most significant bit (MSB) first (bit 15), perform the following steps:
   a. MOSI = bit to be sent. These bits are the data that is being written to the Slot-Select Register.
   b. Pull SPICLK low.
   c. Release SPICLK high. This rising edge clocks the data.
5. Release INTR* high to assert the SS* line of the module whose slot number was written to Slot 0. When no communications are taking place, write zero to the Slot-Select Register to prevent accidental writes.



Name	Description	Minimum	Maximum
T1	INTR* low to SS* disabled	—	200 ns
T2	INTR* low to first rising edge on SPICLK	75 ns	—
T3	Last rising edge on SPICLK to INTR* high	250 ns	—
T4	INTR* high to SS* enabled	—	350 ns

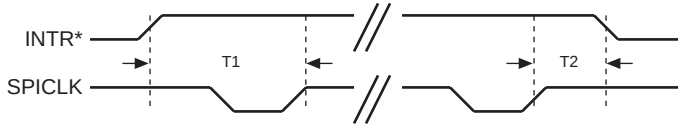
Figure 4. Slot-Select Timing Diagram

Writes to Slot 0 Registers

In addition to the Slot-Select Register, there are two other registers in Slot 0. They are the Hardscan Control Register (HSCR) and the first-in-first-out (FIFO) Register. These registers are used to program Slot 0 to help control scanning operations. Refer to your SCXI chassis register-level programmer manual for register descriptions; for a discussion regarding timing requirements on the scanning operations, see the *SCANCON Timing Requirements and Specifications* section of your SCXI chassis register-level programmer manual.

To write to the HSCR or the FIFO Register, perform the steps below. See Figure 5 for timing specifications.

1. If you are writing to the HSCR, select Slot 13 by following the Slot-Select Procedure. If you are writing to the FIFO Register, select Slot 14 by following the Slot-Select Procedure.
2. For each bit, starting with the MSB first (bit 7 for the HSCR, bit 15 for the FIFO Register), perform the following steps:
   a. MOSI = bit to be sent.
   b. Pull SPICLK low.
   c. Release SPICLK high. This rising edge clocks the data.
3. Pull INTR* low to latch the register data, and establish conditions for writing a new slot-select number to the Slot-Select Register.
4. If you do not select another slot, write zero to the Slot-Select Register. If you do select another slot, start at step 4 of the previous section, *Slot-Select Procedure*.



Name	Description	Minimum	Maximum
T1	INTR* high to first rising edge on SPICLK	75 ns	—
T2	Last rising edge on SPICLK to INTR* low	250 ns	—

Figure 5. Slot 0 Register Writes Diagram

Module Types and Communication Protocols

There are two types of modules from a communication point of view—those with an address handler, and those without an address handler.

Class I Modules

A class I module contains two registers, a Configuration Register that receives data on the MOSI line, and a Module ID Register that puts out data on the MISO line. The Configuration Register may be any number of bits; you should, however, limit the bit length to 32 bits. If more are needed, split the bits into multiple configuration registers and make the module a class II module. The Module ID Register must be four bytes long. The Module ID Register must clock data out, MSB first for each byte, and send the least significant byte first. For example, a Module ID of 384 would be sent as `10000000 00000001 00000000 00000000`, where the first `1` is the first bit sent.

The Configuration Register should receive data only when SS* is low and D*/A is low. The Module ID Register should clock out data when SS* is low, independent of the state of D*/A.

After the four bytes of Module ID have been sent out, the module may send out erroneous data. Deasserting the SS* line high should cause the Module ID Register to reinitialize. Figure 6 shows the class I module structure.

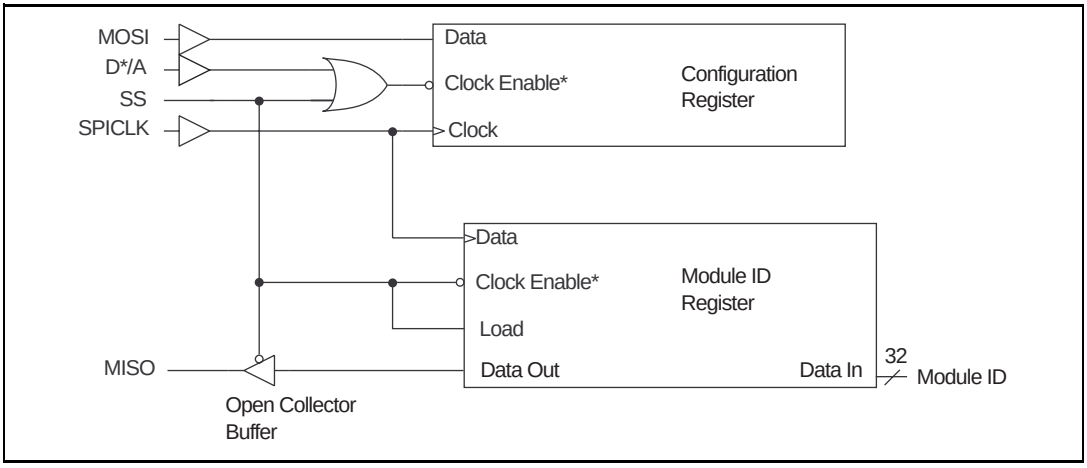
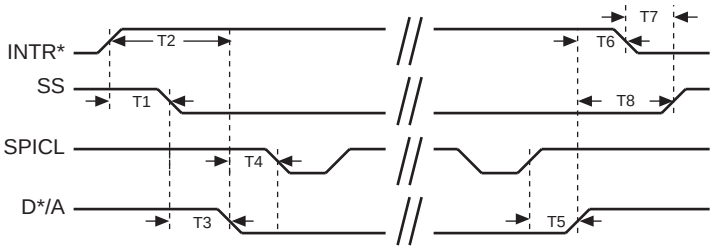


Figure 6. Class I Module Structure Diagram

To write to a class I module Configuration Register, follow the steps below. Refer to Figure 7 for timing specifications.

1. Select the slot of the desired module following the *Slot-Select Procedure* earlier in this document.
2. Pull D*/A low to write data to the Configuration Register.
3. For each bit to be written, perform the following steps:
   a. MOSI = bit to be sent.
   b. Pull SPICLK low.
   c. Release SPICLK high. This rising edge clocks the data.
4. Pull INTR* low to deassert the SS* line and establish conditions for writing a new slot-select number to the Slot-Select Register.
5. If you do not select another slot, you should write zero to the Slot-Select Register. If you do select another slot, start at step 4 of the *Slot-Select Procedure* earlier in this document.



Name	Description	Master	Slave
T1	INTR* high to SS* enabled	350 ns max	—
T2	INTR* high to D*/A low	450 ns min	—
T3	SS* enabled to D*/A low	—	80 ns min
T4	D*/A low to first falling edge on SPICLK	100 ns min	80 ns min
T5	Last rising edge on SPICLK to D*/A high	250 ns min	80 ns min
T6	D*/A high to INTR* low	350 ns min	—
T7	INTR* low to SS* disabled	200 ns max	—
T8	D*/A high to SS* disabled	—	80 ns min

Figure 7. Class I Timing Diagram

Class II Modules

A class II module has an address handler, a 16-bit register that is written to when D*/A is high and SS* is low. The address in the address handler indicates which of 65,536 possible locations on the module will be accessed by the master when the D*/A line is low, indicating a data write instead of an address write. The address handler should be constructed so that if more than 16 bits are written, the leading bits are thrown out and the address handler only retains the last 16 bits.

A class II module must have a Module ID Register located at address zero. The Module ID Register must be four bytes long. Data must be clocked out MSB first for each byte, with the least significant byte being sent first. For example, a Module ID of 384 would be sent as `10000000 00000001 00000000 00000000`, where the first `1` is the first bit sent.

The Module ID Register should clock out data when it is selected by the address handler. After the four bytes of the Module ID have been sent out, the Module ID Register may send out erroneous data. Deselection by the address handler should cause the Module ID Register to reinitialize. Locations accessed by the address handler can be of many varieties; Registers, EEPROMs, microcontrollers, and so on. When a peripheral is a simple register whose information must also be stored in memory on a remote computer, the register should be limited to 32 bits in length. Figure 8 shows the class II module structure.

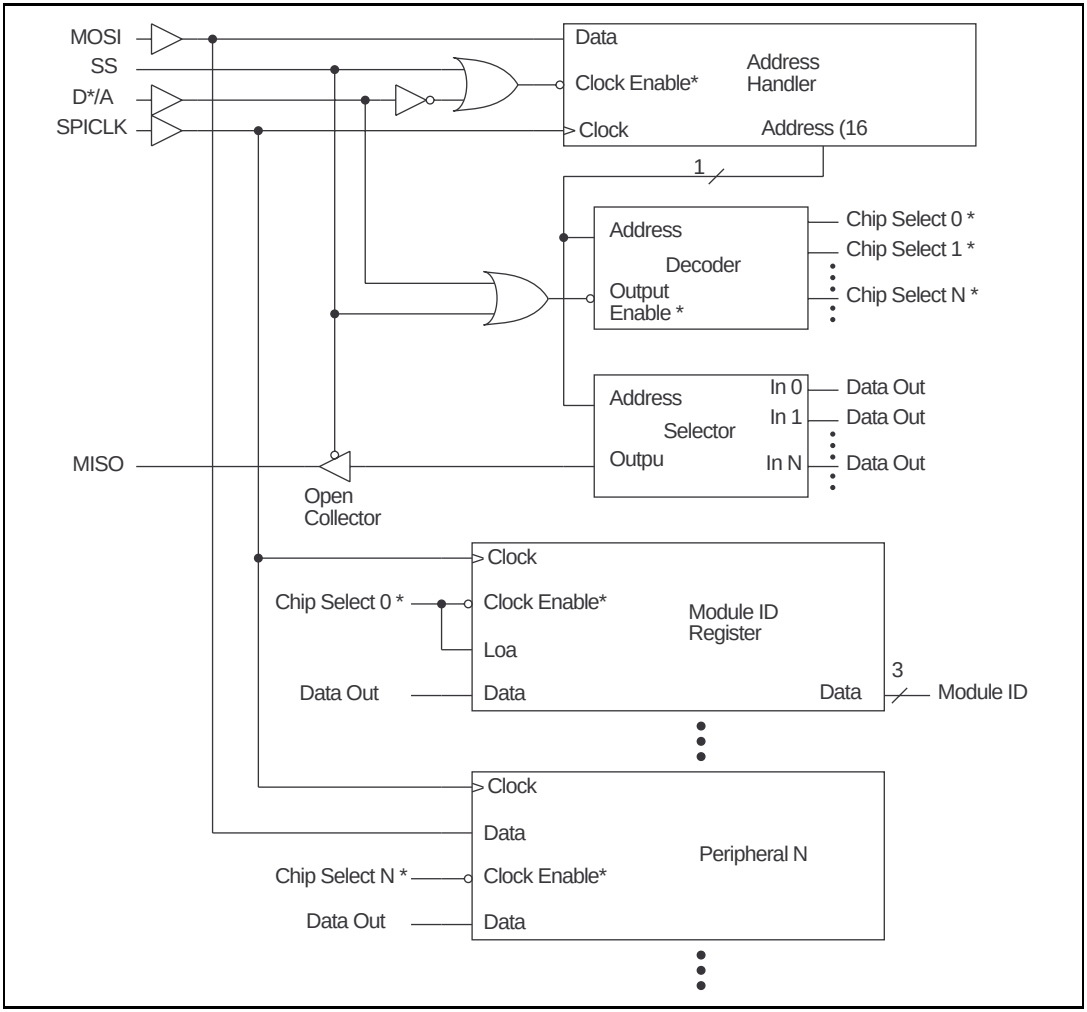
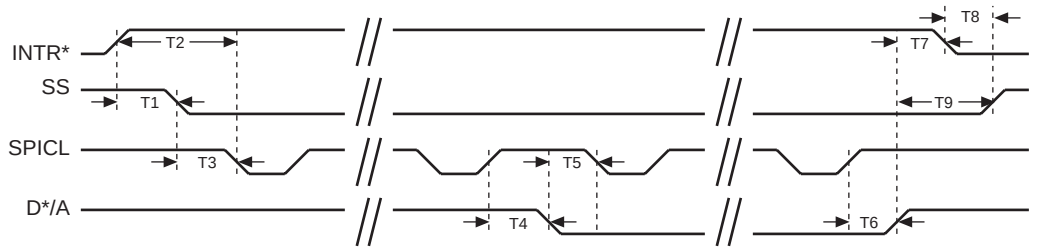


Figure 8. Class II Module Structure Diagram

To communicate with a class II module, perform the steps below. Refer to Figure 9 for timing specifications.

1. Select the slot of the desired module following the *Slot-Select Procedure* earlier in this document.
2. Write the 16-bit address of the peripheral to the class II module with which communications will take place. For each address bit, MSB first, perform the following steps:
   a. MOSI = bit to be sent.
   b. Pull SPICLK low.
   c. Release SPICLK high. This rising edge clocks the data.

3. Pull D*/A low to indicate that data will be transmitted instead of an address. Notice that depending on the complexity of the peripheral, some of the *data* information that is sent may be address information for the peripheral. However, the chassis does not know this and so this information is still referred to as *data*.
4. Communicate with the peripheral. The specifics of how this is done depends on the peripheral. Some peripherals may have simple registers like the Configuration Register in a class I module, whereas others may be EEPROMs or microcontrollers with more elaborate protocols.
5. To talk to a different peripheral on the same slot, release D*/A high and proceed from step 2 of this section. To talk to a different module, start at step 1 of this section or step 1 of the section, *Class I Modules*, whichever is appropriate.



Name	Description	Master	Slave
T1	INTR* high to SS* enabled	350 ns max	—
T2	INTR* high to first falling edge on SPICLK	450 ns min	—
T3	SS* enabled to first falling edge on SPICLK	—	80 ns min
T4	Last rising edge on SPICLK to D*/A low	350 ns min	80 ns min
T5	D*/A low to first falling edge on SPICLK	100 ns min	80 ns min
T6	Last rising edge on SPICLK to D*/A high	250 ns min	—
T7	D*/A high to INTR* low	350 ns min	—
T8	INTR* low to SS* disabled	200 ns max	—
T9	D*/A high to SS* disabled	—	80 ns min

Figure 9. Class II Timing Diagram

Module ID Protocol

The procedure for reading the Module ID of a slot follows. Before reading the ID, it is not known whether the module is class I or class II. The timing specifications for this procedure are equivalent to those discussed in the previous section, *Class II Modules*.

1. Select the slot of the desired module following the *Slot-Select Procedure* earlier in this document.
2. Write 32 zeros to the module and read the Module ID that is present on the MISO line.
3. If the Module ID is all ones, go to step 4; otherwise, you have read the Module ID of a class I module and should go to step 7.
4. Pull D*/A low.
5. Write 32 bits of anything to the module and read the Module ID that is present on the MISO line.
6. If the Module ID was all ones, the slot is empty. Otherwise, you have read the Module ID of a class II module.
7. Deselect the slot.

SCANCON Timing Requirements and Specifications

Slot 0 contains timing circuitry that you can use to choose one module at a time during a scanning operation. Program the FIFO Register and HSCR to set up a scan list. This scan list is a list of modules, and for each entry, a count to indicate how long the module is selected. After you program Slot 0, the slot that corresponds to the first entry is *chosen*, meaning that its SCANCON pin is active or low. Slot 0 counts falling edges on TRIG0. After the number of falling edges on TRIG0 matches the count for the current scan list entry, the next entry becomes active, and the SCANCON for that module is asserted.

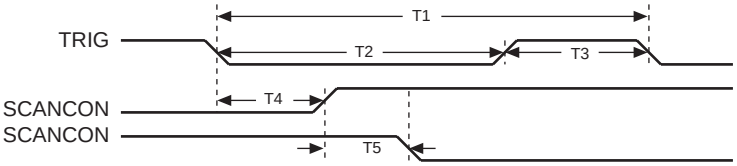
The timing relations between TRIG0 and SCANCON follows. For more information on the programming operation of the hardscan circuitry, refer to the SCXI chassis user manual.

There are two different modes of SCANCON operation from a timing point of view. In one case, there is a gap between the switching of the SCANCON signals. This mode is useful for two reasons:

- First, if consecutive scan list entries are for the same module, the SCANCON line pulses high between entries, indicating to the module that the scan list has advanced an entry.
- Second, when modules that are multiplexing their outputs to the analog bus use the hardscan circuitry as an enable signal, the gap ensures that during switching, two modules do not simultaneously drive the bus. This situation could easily occur if different modules have switches with different delay times. If you output-protect the outputs of the drivers, no damage occurs, but the driver contention could make an amplifier oscillate or ring, thus producing bad results.

In the other case, there is no gap between transitions, and if consecutive scan list entries are for the same module, SCANCON remains low between the transition. Use this mode when it is necessary to hold SCANCON low for more than the 128 counts that is the maximum for a

scan list entry. Notice that in this case, to get SCANCON to go high on one module, you need an entry for a different module. On the SCXI-1000, FIFO Register entries can be for only one of the four slots. On the SCXI-1001, FIFO Register entries can be for a dummy slot, so that no SCANCON is asserted. Figure 10 shows the timing for the SCANCON and TRIG0 signals.



Name	Description	Driver
T1	Period of clock on TRIG0	1.3 µs min
T2	Low time of TRIG0	250 ns min
T3	High time of TRIG0	
	(Driver)	400 ns min
	(Receiver)	150 ns min
T4	Delay from TRIG0 falling edge to current SCANCON disabled	250 ns max
T5	Delay from current SCANCON disabled to next SCANCON enabled with gap	100 ns min 350 ns max
	Without gap (no break if SCANCONs are the same)	–25 ns min +25 ns max

Figure 10. SCANCON and TRIG0 Timing Diagram

Note ***Driver refers to the module that drives TRIG0, and Receiver refers to any other module that is listening to TRIG0.***